WHAT IS CLAIMED IS:

1. A semiconductor memory element comprising:

a thin film region formed over an insulator and made of a semiconductor;

first and second low-resistance regions,

wherein said thin film region has a first end portion connected with said first low-resistance region, and

wherein said thin film region has a second end portion connection with said second low-resistance region; and

a control electrode for controlling said thin film region, wherein said control electrode entirely covers said thin film region.

2. A semiconductor memory element comprising:

a thin film region formed over an insulator and made of a semiconductor;

first and second low-resistance regions,

wherein said thin film region has a first end portion connected with said first low-resistance region, and

wherein said thin film region has a second end portion connected with said second low-resistance region, and

a control electrode for controlling said thin film region,

wherein said first and second low-resistance regions are formed over said insulator.

3. A semiconductor memory element for storing at least 2 bits, comprising:

first and second thin film regions formed over an insulator and made of a semiconductor;

first and second low-resistance regions made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said second low-resistance region,

wherein said second thin film region has its one end portion connected with said first low-resistance region, and

wherein said second thin film region has its other end portion connected with said second low- resistance region;

a first control electrode for controlling said first thin film region; and

a second control electrode for controlling said second thin film region.

4. A semiconductor memory element for storing at least 2 bits, comprising:

first and second thin film regions formed over an insulator and made of a semiconductor;

a first low-resistance region made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side;

second and third low-resistance regions made thicker than said thin film region,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said second low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region, and

wherein said second thin film region has a second end portion connected with said third low- resistance region;

a first control electrode for controlling said first thin film region; and

a second control electrode for controlling said second thin film region.

5. A semiconductor memory element for storing at least 2 bits, comprising:

first and second thin film regions formed over an insulator and made of a semiconductor;

first, second, third and fourth low-resistance regions made thicker than said thin film regions,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said second low-resistance region,

wherein said second thin film region has a first end portion connected with said third low-resistance region, and

wherein said second thin film region has a second end portion connected with said fourth low- resistance region; and

a common control electrode for controlling said first and second thin film regions.

6. A semiconductor memory element for storing at least 2 bits, comprising:

first and second thin film regions formed over an insulator and made of a semiconductor;

first, second and third low-resistance regions made thicker than said thin film regions,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said second low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region, and

wherein said second thin film region has a second end portion connected with said third low- resistance region; and

a common control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and second thin film regions.

7. A semiconductor memory element for storing at least 2 bits, comprising:

first and second thin film regions formed over an insulator and made of a semiconductor;

a first low-resistance region made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side;

second and third low-resistance regions made thicker than said thin film region,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said second low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region, and

wherein said second thin film region has a second end portion connected with said third low- resistance region; and

a common control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and second thin film regions,

wherein a longitudinal direction of said first low-resistance region and a longitudinal direction of said control electrode are generally in parallel.

8. A semiconductor memory element for storing at least 4 bits, comprising:

first, second, third and fourth thin film regions formed over an insulator and made of a semiconductor;

first, second, third and fourth low-resistance regions made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side at least two times longer than a shorter side,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said second low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region,

wherein said second thin film region has a second end portion connected with said second low- resistance region,

wherein said third thin film region has a first end portion connected with said third low-resistance region,

wherein said third thin film region has a second end portion connected with said fourth low-resistance region,

wherein said fourth thin film region has a first end portion connected with said third low-resistance region, and

wherein said fourth thin film region has a second end portion connected with said fourth low- resistance region;

a first control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and third thin film regions; and

a second control electrode formed into a substantially rectangular shape having a longer side at least two times longer than a shorter side for controlling said second and fourth thin film regions.

9. A semiconductor memory element for storing at least 4 bits, comprising:

first, second, third and fourth thin film regions formed over an insulator and made of a semiconductor;

first and second low-resistance regions made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side;

third and fourth low-resistance regions made thicker than said thin film regions,

wherein said first thin film region has a first one end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said third low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region,

wherein said second thin film region has a second end portion connected with said fourth low- resistance region,

wherein said third thin film region has a first end portion connected with said second low-resistance region,

wherein said third thin film region has a second end portion connected with said third low-resistance region,

wherein said fourth thin film region has a first end portion connected with said second low-resistance region, and

wherein said fourth thin film region has a second end portion connected with said fourth low- resistance region;

a first control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and third thin film regions; and

a second control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said second and fourth thin film regions.

10. A semiconductor memory element as set forth in claim 9, wherein said third and fourth low-resistance regions are connected with said third and fourth low- resistance regions by an identical material.

11. A semiconductor memory element for storing at least 4 bits, comprising:

first, second, third and fourth thin film regions formed over an insulator and made of a semiconductor;

a first low-resistance region made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side;

second, third, fourth and fifth low-resistance regions made thicker than said thin film region,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said second low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region,

wherein said second thin film region has a second end portion connected with said third low- resistance region,

wherein said third thin film region has a first end portion connected with said first low-resistance region,

wherein said third thin film region has a second end portion connected with said fourth low-resistance region,

wherein said fourth thin film region has a first end portion connected with said first low-resistance region, and

wherein said fourth thin film region has a second end portion connected with said fifth low- resistance region;

a first control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and third thin film regions; and

a second control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said second and fourth thin film regions.

12. A semiconductor memory element for storing at least 4 bits, comprising:

first, second, third and fourth thin film regions formed over an insulator and made of a semiconductor;

first and second low-resistance regions made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side;

third and fourth low-resistance regions made thicker than said thin film regions,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said third low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region,

wherein said second thin film region has a second end portion connected with said fourth low- resistance region,

wherein said third thin film region has a first end portion connected with said second low-resistance region,

wherein said third thin film region has a second end portion connected with said third low-resistance region,

wherein said fourth thin film region has a first end portion connected with said second low-resistance region, and

wherein said fourth thin film region has a second end portion connected with said fourth low- resistance region;

a first control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and second thin film regions; and

a second control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said third and fourth thin film regions.

13. A semiconductor memory element as set forth in claim 11, further comprising:

fifth and sixth low-resistance regions formed of a layer different from that of said third and fourth low-resistance regions,

wherein said fifth low-resistance region is connected with said third low-resistance region,

wherein said sixth low-resistance region is connected with said fourth low-resistance region, and

wherein said fifth low-resistance region and said sixth low-resistance region extend in a direction parallel to one another.

14. A semiconductor memory element for storing at least 4 bits, comprising:

first, second, third and fourth thin film regions formed over an insulator and made of a semiconductor;

a first low-resistance region made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side;

second, third, fourth and fifth low-resistance regions made thicker than said thin film region,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said second low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region,

wherein said second thin film region has a second end portion connected with said third low- resistance region,

wherein said third thin film region has a first end portion connected with said first low-resistance region,

wherein said third thin film region has a second end portion connected with said fourth low-resistance region,

wherein said fourth thin film region has a first end portion connected with said first low-resistance region, and

wherein said fourth thin film region has a second end portion connected with said fifth low- resistance region;

a first control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and second thin film regions; and

a second control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said third and fourth thin film regions.

15. A semiconductor memory element as set forth in claim 14, further comprising:

sixth and seventh low-resistance regions formed of a layer different from that of said second and third low-resistance regions,

wherein said sixth low-resistance region is connected with said second low-resistance region,

wherein said seventh low-resistance region is connected with said third low-resistance region, and

wherein said sixth low-resistance region and said seventh low-resistance region extend in parallel.

16. A semiconductor memory element for storing at least 4 bits, comprising:

first, second, third and fourth thin film regions formed over an insulator and made of a semiconductor;

first, second, third, fourth, fifth and sixth low-resistance regions made thicker than said thin film regions,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said third low-resistance region,

wherein said second thin film region has a first end portion connected with said second low-resistance region,

wherein said second thin film region has a second end portion connected with said fourth low- resistance region,

wherein said third thin film region has a first end portion connected with said third low-resistance region,

wherein said third thin film region has a second end portion connected with said fifth low-resistance region,

wherein said fourth thin film region has a first end portion connected with said fourth low-resistance region,

wherein said fourth thin film region has a second end portion connected with said sixth low- resistance region;

a first control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and second thin film regions; and

a second control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said third and fourth thin film regions.

17. A semiconductor memory element for storing at least 4 bits, comprising:

first, second, third and fourth thin film regions formed over an insulator and made of a semiconductor;

first and second low-resistance regions made thicker than said thin film regions and formed into a substantially

rectangular shape having a longer side that is at least two times longer than a shorter side;

third, fourth, fifth and sixth low-resistance regions made thicker than said thin film regions,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said third low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region,

wherein said second thin film region has a second end portion connected with said fourth low- resistance region,

wherein said third thin film region has a first end portion connected with said second low-resistance region,

wherein said third thin film region has a second end portion connected with said fifth low-resistance region,

wherein said fourth thin film region has a first end portion connected with said second low-resistance region,

wherein said fourth thin film region has a second end portion connected with said sixth low- resistance region;

a first control electrode formed into a substantially rectangular shape having a longer side that is

at least two times longer than a shorter side for controlling said first and third thin film regions; and

a second control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said second and fourth thin film regions.

18. A semiconductor memory element for storing at least 4 bits, comprising:

first, second, third and fourth thin film regions formed over an insulator and made of a semiconductor;

first and second low-resistance regions made thicker than said thin film regions and formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side;

third, fourth, fifth and sixth low-resistance regions made thicker than said thin film regions;

seventh and eighth low-resistance regions made of a layer different from that of said third, fourth, fifth and sixth low-resistance regions,

wherein said first thin film region has a first end portion connected with said first low-resistance region,

wherein said first thin film region has a second end portion connected with said third low-resistance region,

wherein said second thin film region has a first end portion connected with said first low-resistance region,

wherein said second thin film region has a second end portion connected with said fourth low- resistance region,

wherein said third thin film region has a first end portion connected with said second low-resistance region,

wherein said third thin film region has a second end portion connected with said fifth low-resistance region,

wherein said fourth thin film region has a first end portion connected with said second low-resistance region,

wherein said fourth thin film region has a second end portion connected with said sixth low- resistance region;

a first control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said first and second thin film regions; and

a second control electrode formed into a substantially rectangular shape having a longer side that is at least two times longer than a shorter side for controlling said third and fourth thin film regions,

wherein said third low-resistance region is connected with said seventh low-resistance region,

wherein said fourth low-resistance region is connected with said eighth low-resistance region,

wherein said fifth low-resistance region is connected with said seventh low-resistance region, and

wherein said sixth low-resistance region is connected with said eighth low-resistance region.

19. A semiconductor memory element as set forth in claim 1, wherein said low-resistance regions are formed over said insulator.

20. A semiconductor memory element as set forth in claim 2, wherein in an information writing or erasing operation, any of said low-resistance regions takes a negative potential.

21. A semiconductor memory element as set forth in claim 1, wherein said low-resistance regions are connected with a wiring line of another layer.

22. A semiconductor memory element as set forth in claim 1, wherein said thin film region is shaped to have a projection in a horizontal direction with respect to a film thickness.

23. A semiconductor memory element as set forth in claim 1, wherein said thin film region includes a plurality of lines having each of their first and second ends connected with an identical one of said low-resistance regions and controlled by a common control electrode.

24. A semiconductor memory element as set forth in claim 1, wherein said thin film region is made of polycrystalline silicon having a thickness of 5 nm or less.

25. A semiconductor memory element as set forth in claim 3, wherein the information of a plurality of bits is erased or written in a block by changing the potential of a semiconductor substrate.

26. A semiconductor memory element as set forth in claim 1, further comprising a second control electrode in addition to said control electrode for controlling said thin film region.

27. A semiconductor memory element having a stacked structure of said semiconductor memory element as set forth in claim 1.

28. A semiconductor memory which consists of semiconductor memory elements as set forth in claim 1, having at least one pair of dummy low-resistance upper regions, corresponding to a data line and a source line, which are not used for a read operation.

29. A semiconductor memory which consists of semiconductor memory elements as set forth in claim 1, having at least one dummy control electrode, corresponding to a word line, which is not used for a write or erase operation.

30. A semiconductor memory as set forth in claim 1, having at least one control electrode, corresponding to a word line, which is not used for write or erase operation.

31. A method of forming a memory element for use in a large-scale integrated circuit comprising the steps of:

forming, on a silicon substrate, an insulating layer;

depositing a silicon nitride film over the insulating layer;

depositing a highly-doped n-type polycrystalline silicon layer over the silicon nitride film to form at least two low-resistance regions;

depositing a layer of amorphous silicon to form a thin film region over the low-resistance regions and a portion of the silicon nitride film;

depositing a layer of silicon dioxide over the thin film and the silicon nitride film; and

depositing a layer of highly-doped n-type polycrystalline silicon over the layer of silicon dioxide in order to form a control electrode.

32. The method according to claim 1, wherein the control electrode is formed so as to completely cover the thin film region.

33. The method according to claim 2, wherein the memory element is capable of storing at least two bits.

34. A semiconductor memory according to claim 1, wherein the thin film region contains first and second low potential regions, wherein the first low potential region defines a current path under low current conditions and the second low potential region defines an isolated region, and

wherein when sufficiently high voltage is applied to the control electrode to generate a local electric field between the first low potential region and the second low potential region, at least one electron is transferred from the first low potential region to the second low potential region where the electron is then trapped.

35. A semiconductor memory according to claim 34, wherein when a sufficiently low voltage is applied to the control electrode, said at least one electron leaves the second low potential region.

36. A semiconductor memory according to claim 35, wherein said thin film is formed from ultra-thin polycrystalline silicon.